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# Design and Implementation of Search and Tracking Modules of GPS Receiver on FPGA

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## ABSTRACT

*GPS Receiver is a topic of great importance in navigation, because of having many applications such as aviation, military, surveying and marine are some of the applications. In this work , the small overview of the GPS, its structure and working is presented and how the satellite signals are being transmitted. The implementation of search and tracking module is presented and are modeled in Hardware Description Language(VHDL).*

*Keywords–GPS, GPS Receiver, Navigation, FPGA*

## I. INTRODUCTION

Global Positioning System (GPS) is a global satellite navigation system. It provides with the information of accurate time and exact position to users anywhere on earth. Currently, GPS is not only used for the military applications but now also used for the civil applications. GPS system is used for navigation and positioning. Meanwhile, GPS can also be exploited as the part of the more complex system or incorporated into the more complex system to provide time and location information [1].

The GPS constellation is normally consists of 24 satellites which orbit the earth approximately 20,000km above the earth's surface. They orbit the earth twice a day. Initially the satellite constellation was designed for 24 satellites, but currently it has more than 30 satellites. GPS Receivers is a topic of great importance because of the wide range of applications in many fields such as aviation, surveying, security, science and defense to name a few.

Satellites uses different signals to propagate through for military and civilian use. The most frequently or commonly used civilian signal is the L1 signal which is used to broadcast the navigation message or the GPS

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message. The navigation message is composed of the satellite clock, GPS time, health of the satellite, Ephemeris data and Almanac data. Satellite position with respect to earth can be calculated by using these parameters.

The brief contents of the section has been provided below: section II gives the brief idea about the GPS signals; section III provides the general idea about the GPS receiver; section IV presents the implementation of the modules; section V presents the results and section VI presents the conclusion.

## II. OVERVIEW OF THE GPS SIGNALS

GPS is a global satellite navigation system which provides the user with time and location information. All GPS satellites broadcast the signals in the same frequency but use different ranging codes with low cross correlation properties [2]. GPS transmits its civilian signal L1 hving carrier frequency of 1575.42 MHz. Each GPS satellite (or transmitter) has a unique spreading gold code (C/A code) that is orthogonal to all the other satellites codes [3]. Each satellite multiplies C/A code which is unique to each one of them with its own navigation message. This gold code (C/A code) has a period of 1023 chips. It has a bit rate of 1.023 Mbps.

C/A codes belongs to the family of Gold pseudo-random codes. Due to their particular correlation properties these codes are very useful. When these codes are in phase their autocorrelation is maximum and the autocorrelated code phase differ by more than a chip then it is negligible. By correlating the GPS incoming signal with a locally generated replica of the signal, we can obtained the navigation message.

The function of the search module is to find the CA code phase and the carrier frequency. When the satellites carrier frequency and CA code phase is found, these information is forwarded to the tracking module. The function of the tracking module is to monitor the given signal in CA code phase and carrier frequency.

## III. GPS RECEIVER

The block diagram of the GPS receiver is shown in Fig.1 [4].It consists of the front end module which process the GPS signal so that it can be subsequently processed in real time by the Field Programmable Gate Array FPGA) modules.

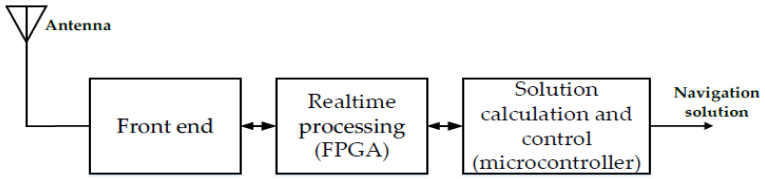


Fig. 1. Block diagram of GPS receiver.

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Block diagram of Front End Module is shown in Fig.2 [4]. The antenna is used to received the RF signal, it is then preamplifed and then filtered in order to reject the image frequency.It is then mixed with a local oscillator signal in order to downconvert it to an intermediate frequency(IF). Then, it is filtered once again to reject the undesired mix products (high order terms) and digitized.

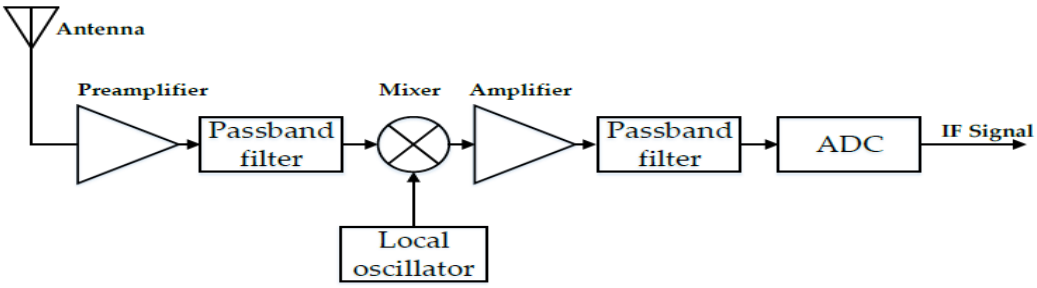


Fig. 2. Block diagram of GPS receiver front end.

The digitized IF signal from Front End Module is then processed in the FPGA module to perform real time operations as search and tracking. The navigation message obtained by the FPGA modules is then passed on to the microcontroller unit to calculate the navigation solution (position and velocity of the vehicle) and perform control operations over the FPGA modules.

## IV. IMPLEMENTATION

1) Search Module

The Search Module correlates the data input signal with the locally generated replicas for different:

- Satellite number
- IF frequency
- CA code phase

The result of this correlation is used to determine if a given satellite is present on the IF signal. The IF frequency and the CA code shift are used as inputs by a tracking module for continuous tracking of that satellite signal in both frequency and CA code phase.

To understand the working of the Search Module certain blocks inside the structure needs to be analysed. The block diagram of the Search Module is shown in Fig. 3 [4].

The block called memModule consist of two first in first out (FIFO) buffers. Everytime, one of the buffers is being written with incoming data and the other buffer stores fresh data samples which can be read and processed by the module. The length of the buffer is enough to receive an entire period of CA code. When the buffer being written is completed, the roles of the buffers are exchanged. In this way,

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many advantages are achieved.Primarily, data samples can be processed at syatem clock frequency( instead of data clock) thus improving processing speed, secondarily there is no need of waiting for the beginning of a new period of the signal.

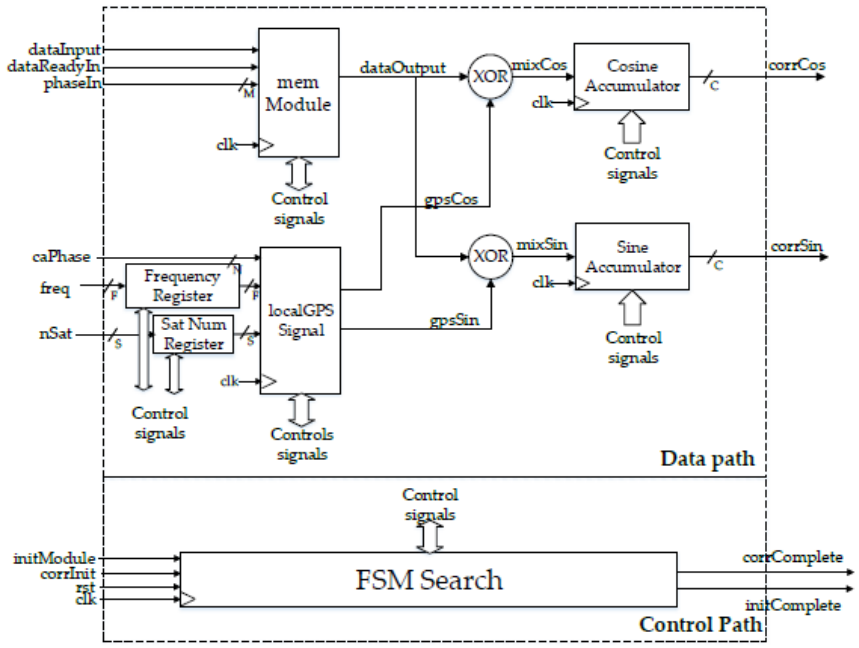


Fig. 3. Block diagram of search module.

The block called localGPSSignal locally generates a GPS signal replica (i.e. a sinewave carrier mixed with CA code) of a given satellite and IF frequency and writes it in an internal memory. Once the signal is reported it can be reproduced at the module output. The localGPSSignalmodule as well as the memModule module allow fast processing of data signals as they can be updated at system clock frequency. Lastly, the two signals (the front end data signal and the local replica) are correlated by the exclusive or (xor) operation and accumulation. So as to attain phase invariance with respect to input carrier phase two branches are calculated in quadrature, one with a cosine replica and the other with a sine replica.

2) Tracking Module

The block diagram of the Tracking Module is shown in Fig. 4 [4]. The control signals for the numerically controlled oscillator (NCO), CA generator, accumulators and output registers blocks in data path are generated by the control path consisting of the Finite State Machine (FSM).

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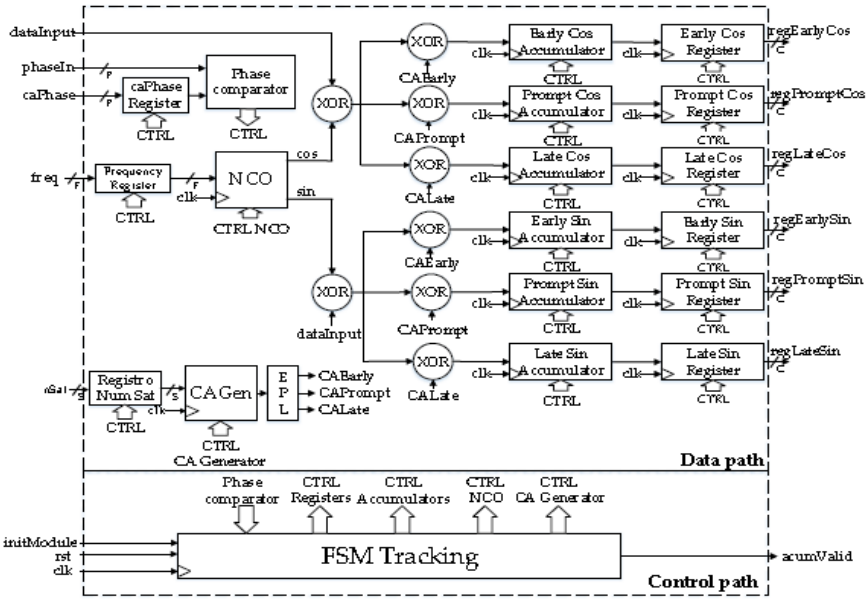


Fig. 4 . Tracking module block diagram.

The data path consists of:

- NCO: The local IF carrier signal whose frequency is resolved by the input frequency is generated by this block.This input is the signed integer value.
- CA generator: A CA code sequence for a given satellite as determined by nSat input is generated by CA generator.This block integrates a shifter that generates three CA code replicas that is CAEarly, CAPrompt and CALate. These replicas are shifted by half a chip between them.
- Accumulators: If the input signal coincides with the local replica then this register increments and if it does not coincide then this register decrements.
- Registers: Signal generation parameters like IF frequency CA code phase and satellite number are stored in the Input registers. The last valid generated value of the accumulators are added to the Output registers.

## V. RESULTS

Search module and tracking module were modelled using Hardware Description Language that is the VHDL. The simulation of the search and tracking module was carried out in the ModelSimSimulater. The results of the search and the tracking modules are given below

1) Search Module Output

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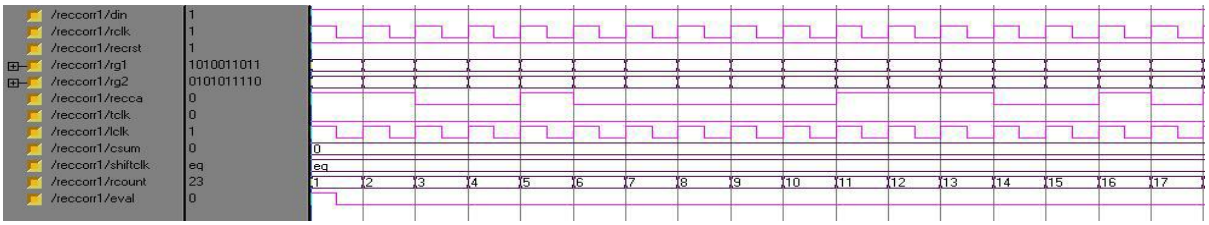
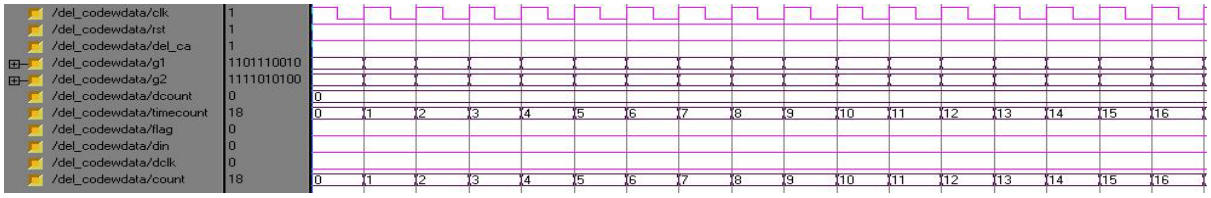



2) Tracking Module Output:




## VI. CONCLUSION

The GPS, what is it could be studied. The structure of GPS, what it consists of.The working of it and also the Navigation Message Format could be studied and analysed. The detailed design of GPS Receiver was analysed and studied. Alsothe search and the tracking modules could be analysed, studied,discribed andimplemented.

## VII. ACKNOWLEDGMENT

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