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Design of a high speed one-bit full adder circuit

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Abstract

Full adder circuit is performing an important role in many system applications such digital signal processors, microprocessors, and arithmetic logic units, etc. In this paper, a hybrid high speed one bit full adder is proposed in 130nm technology. The performance parameters such as propagation delay, power and power delay product are compared with the previous work and found that the proposed one bit full adder gives better propagation delay with respect to other full adder circuits. The delay of the proposed full adder circuit is improved in comparison to CMOS 10T FA, GDI FA, 14T FA and Hybrid FA. All simulations are done at a temperature of 27 ^{0}C by using Mentor Graphics Pyxis EDA tool.

Keywords- CMOS, GDI, Pass transistor logic, Delay, Transmission gate, Power dissipation

1. INTRODUCTION

Full adder circuit is extensively used in arithmetic logic circuits in very large scale integration systems [1]. The explosive development in a portable systems and other processing devices have intensified the research efforts in high speed circuit design. The performance of any digital circuit can be optimised with the help of different logic styles. A full adder circuit can be designed by using different logic styles and structures [2]. A GDI logic based full adder [3] circuit is based on full output swing with ultra low power dissipation. This FA consists of two blocks: one is sum block and the other one is carry block. This adder circuit consists of two XOR gate and one mux circuit. The sum block is implemented by using XOR gate. This circuit alone is not an effective method for very high speed integrated circuit design.

Hybrid FA [4] circuit consists of 16 number of MOS transistors and is designed by XNOR and carry generation module. This full adder circuit provides full swing by using the transmission gate. This circuit provides an optimal value in the propagation delay. However, there is complexity in the circuit implementation and lack of driving capability. 14T FA [5] has a problem in the form of glitches and a subthreshold leakage power component in the output. CMOS 10T FA [6] is designed by using the XOR gate of four transistors and a 2:1 multiplexer by using two transistors.

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2. PROPOSED METHODOLOGY

The proposed full adder circuit represented by three modules is shown in the Fig. 1. Module-1 represents the XOR-XNOR [7] circuit, module-2 generates the SUM signal and module-3 generates the carry out signal.

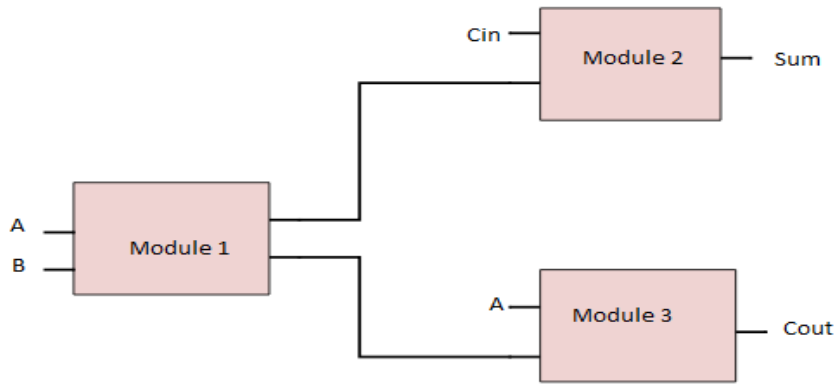

Fig. 1. Block level representation of the proposed full adder

Fig. 2 shows the complete circuit diagram of the proposed full adder. Module 1 consists of XOR-XNOR gates [8, 9] and is designed by using GDI technique to achieve the better delay. In this module, eight transistors are used to generate the XOR-XNOR functions. This module is giving the full swing with low voltage. This module is connected with module 2 and module 3 for producing sum and carry signal. Modules 2 and 3 are based on transmission logic function [10], which provides a better performance in terms of lower propagation delay. In module 2, four transistors are used while in module 3, four transistors are used. Sum and Carry functions are generated through module 2 and module 3 respectively.

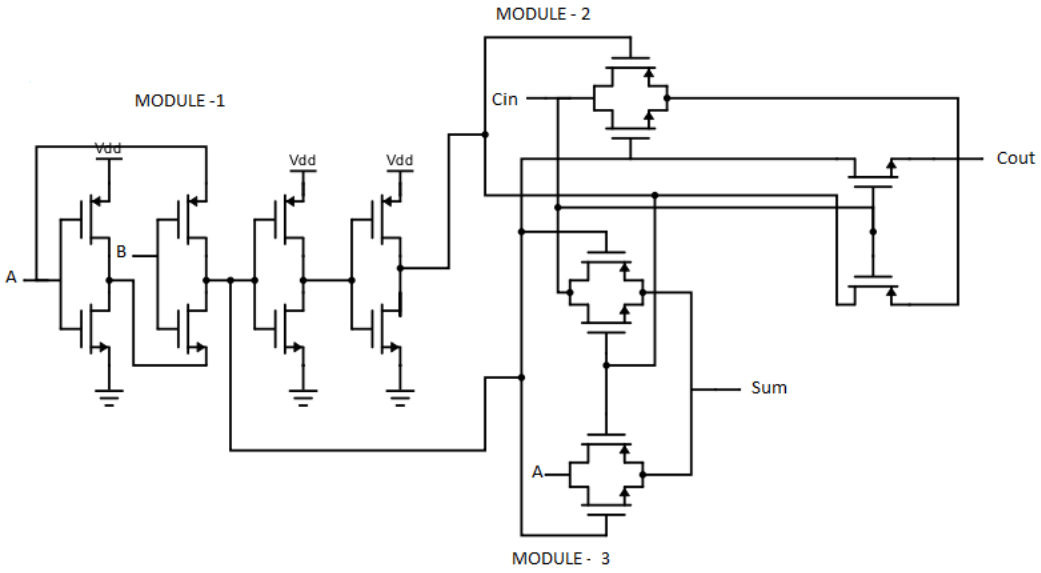

Fig. 2. Circuit diagram of the proposed full adder

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3. RESULTS AND DISCUSSION

The full adder circuit is designed and simulated by using Mentor Graphics Pyxis EDA Tools in 130 nm technology and at temperature of 27 ^{0}C. The designed circuit is analysed and compared with some previous related works such as CMOS 10T FA, GDI FA, 14T FA, and Hybrid FA on the basis of performance parameters such as propagation delay, power dissipation, and power delay product. Tables 1-6 show the performance comparison of the proposed FA with some previous FA design. Fig. 3 shows the input and output waveform of the proposed full adder circuit at V_{DD} = 1.2 V.

Table 1. Performance comparison at V_{DD} = 0.6 V

FA Design	Power dissipation	Delay	Power delay product
CMOS 10 T FA [6]	3.432pw	61.659 ns	223.267 *10^{-21} Ws
GDI FA [3]	16.214 uw	6.9309 ns	116.458 *10^{-15} Ws
14 T FA [5]	488.052 pw	11.052 ns	5368 *10^{-21} Ws
Hybrid FA [4]	31.423 uw	15.609 ns	490.481 *10^{-15} Ws
Proposed FA	7.970 uw	2.72 ns	15.943 *10^{-15} Ws

Table 2. Performance comparison at V_{DD} = 0.8 V

FA Design	Power dissipation	Delay	Power delay product
CMOS 10 T FA [6]	6.218 pw	61.643 ns	383.296 *10^{-21} Ws
GDI FA [3]	73.634 uw	8.026 ns	590.986 *10^{-15} Ws
14 T FA [5]	733.717 pw	9.414 ns	6904.211 *10^{-21} Ws
Hybrid FA [4]	126.057 uw	29.192 ns	3679.85 *10^{-15} Ws
Proposed FA	9.831 uw	3.952 ns	38.852 * 10^{-15} Ws

Table 3.Performance comparison at V_{DD} = 1V

FA Design	Power dissipation	Delay	Power delay product
CMOS 10 T FA [6]	9.5807 pw	87.045 ns	883.895 *10^{-21} Ws
GDI FA [3]	184.085 uw	8.213 ns	1511.52 *10^{-15} Ws
14 T FA [5]	1.034 nw	9.797 ns	5368 *10^{-18} Ws
Hybrid FA [4]	296.593 uw	16.621 ns	4923.44 *10^{-15} Ws
Proposed FA	79.098 mw	4.764 ns	376.901 *10^{-12} Ws

Table 4.performance comparison at V_{DD} = 1.2 V

FA Design	Power dissipation	Delay	Power delay product
CMOS 10 T FA [6]	13.668 pw	37.531 ns	512.960 *10^{-21} Ws
GDI FA [3]	213.231 uw	8.341 ns	1778.559 *10^{-15} Ws
14 T FA [5]	1.399 nw	9.887 ns	132.386 *10^{-18} Ws
Hybrid FA [4]	549.748 uw	16.633 ns	9077.98 *10^{-15} Ws
Proposed FA	174.436 mw	4.786 ns	833.774 * 10^{-12} Ws

Table 4. Performance comparison at V_{DD} = 1.8V

FA Design	Power dissipation	Delay	Power delay product
CMOS 10 T FA [6]	30.332 pw	39.999 ns	1199.975 * 10^{-21} Ws
GDI FA [3]	264.311 uw	8.345 ns	2205.675 *10^{-15} Ws
14 T FA [5]	3.0145 nw	9.857 ns	29.713 *10^{-18} Ws
Hybrid FA [4]	1.763 mw	16.654 ns	29.361 *10^{-12} Ws
Proposed FA	526.086 mw	4.811 ns	2530.099 *10^{-12} Ws

Table 5. Performance comparison at V_{DD} = 2 V

FA Design	Power dissipation	Delay	Power delay product
CMOS 10 T FA [6]	37.374 pw	40.012 ns	1495.408 $*10^{-21}$ Ws
GDI FA [3]	311.431 uw	8.445 ns	2630.034 $*10^{-15}$ Ws
14 T FA [5]	3.7952 nw	9.953 ns	37.773 $*10^{-18}$ Ws
Hybrid FA [4]	2.480 mw	16.624 ns	41.227 $*10^{-12}$ Ws
Proposed FA	823.076 mw	4.853 ns	3994.387 $*10^{-12}$ Ws

Table 6. Performance comparasion at V_{DD}= 3 V

FA Design	Power dissipation	Delay	Power delay product
CMOS 10 T FA [6]	83.818 pw	40.013 ns	3353.809 * 10^{-21} Ws
GDI FA [3]	4.941 mw	8.634 ns	42.660 $*10^{-12}$ Ws
14 T FA [5]	11.143 nw	9.9685 ns	111.073 $*10^{-18}$ Ws
Hybrid FA [4]	7.206 mw	16.641 ns	119.917 $*10^{-12}$ Ws
Proposed FA	924.063 mw	4.953 ns	4576.884 $*10^{-12}$ Ws

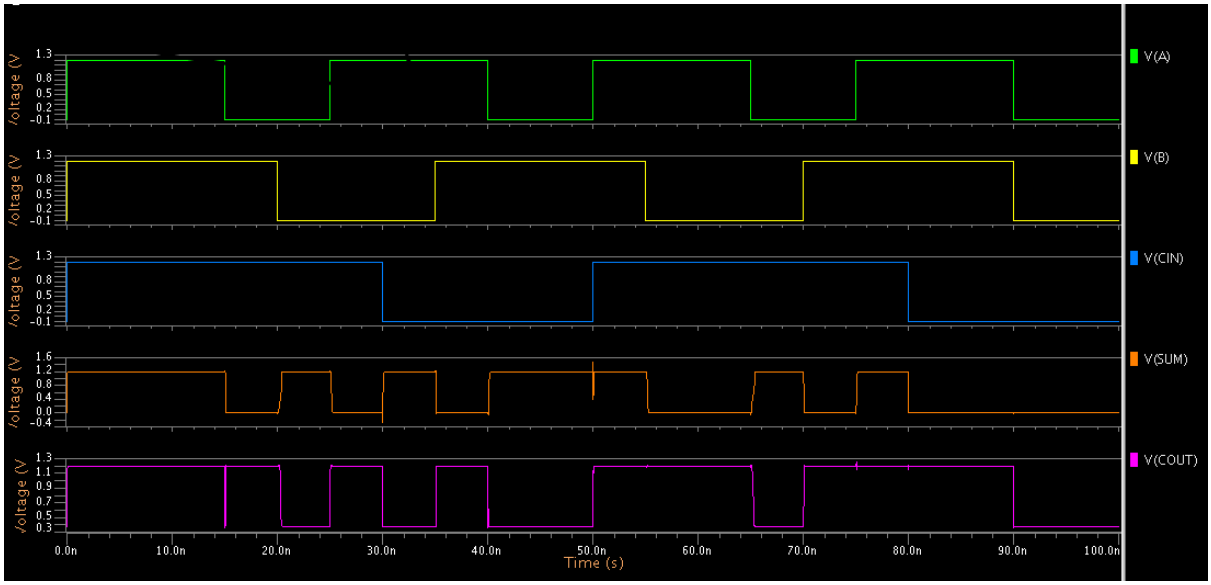

Fig. 3. Input and output waveform of proposed FA circuit at V_{DD} = 1.2 V

4. CONCLUSION

The proposed full adder circuit has an improvement in the propagation delay in comparison with some existing full adder circuits. The designed FA circuit showed better propagation delay while power dissipation was much higher. This proposed FA circuit is suitable for high speed applications.

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