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DESIGN OF DATAPATH ELEMENTS USING IP CORES FOR DEMONSTRATION OF REGISTER RETIMING APPLICATION

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ABSTRACT

IP core based design is highly parametric to enforce code readability and technology independence. Data path elements are integral part of VLSI systems which decides the power dissipation, area consumption and delay of the system. The project mainly focuses to build the data path elements by using standard IP cores available in Xilinx Vivado. Finally the design is verified for power dissipation, area and delay.

Keywords: Zync FPGA, Xilinx vivado

1. INTRODUCTION

Scheming with HDLs has been ordinary practice for 15 years and has led to the growth of well organized and definitive design flow and tools. With the increasing complication of designs two crucial techniques have arose as valuable accompaniment to classical design flow high level synthesis and IP-core based design. The former basically initiate a further, additional abstract level of pre-occupation and the latter tends to change the quantity of granularity at which a outline, or a section of it, is reported. It is worth nothing that spell high-level synthesis has been calculated for a fully prolonged time and has not appreciably assist in padding the productivity gap, the use of IP's.

IP cores are piece of the extending electronic design automation (EDA) industry. In this unit, we will be considering with respect to SRAM based FPGAs. Be transportable, so that it can be pre-owned in any retailer technologies; for example, Xilinx as plug and play. Have processor inclusive parameter file to alter design as needed. Timing contravention can be reduced. Low dynamic and static power can be attained if hard IP blocks are used in the representation. Functionality and staging can be assured. Functionality and performance are countable.

2. BLOCK DIAGRAM OF DATAPATH ELEMENTS:

2.1 REGISTER:

A register is a compact volume of extremely rapid memory that is construct into the CPU[central processing unit] in order to tempo up its performance by providing rapid access to often used values. Registers are the peak of the memory ranking and are the quick procedure for the structure to utilize data. Registers are

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usually sustained by the number of parts they can clutch, for sample 8-bit register means it can store 8-bits of data. It can be of any bit.

2.2 MULTIPLIER:

Multipliers cavort a major role in today's digital signal processing and different other requisitions. Experimenters have attempted and are demanding to represent multipliers which provide high tempo, low power utilization, uniformity of design, less region and compact VLSI implementation.

The ordinary multiplication technique is "add and shift" algorithm. To decrease the number of qualified outcomes to be appended, modified Booth algorithm is one of the majority accepted algorithm. To attain tempo advancement Wallace tree algorithm can be used to decrease the number of sequential adding stages.

2.3 SHIFTER:

A shifter is a combinator circuit with one or spares inputs and an identical number of outputs. The outputs are transferred with regard to the inputs. If unique shift left or shift right is involved, of course gates are not required; such a shift can be consummate with wires. If we represent a shifter that can shift left or right, data should be dispel along the shifter when the shifting is required and throughout it at other times. This enlarges the complication of the control unit.

FIG 2.1 Block diagram of data path elements

3. REGISTER RETIMING CIRCUIT:

Register retiming is a circuit optimization ability that points to condense the clock cycle or decrease circuit region by operational registers ahead or backward in a circuit plan. Unlike extra circuit optimization expertise's, the changes build by retiming span covering register boundaries, thus bemusing the complimenting algorithms. The motivation of register retiming in ceremony is to reposition the registers in such a way that protocol matching algorithms can identify recognize registers.

4. MEHODOLOGY:

Study of various data path elements such of register, adder, substractor, multiplier, divider. Implementing the above listed data path elements by using IP Cores available in Xilinx Vivado. Finally the analyzing the power dissipation, area consumption and delay by XPOWER Xilinx Vivado.

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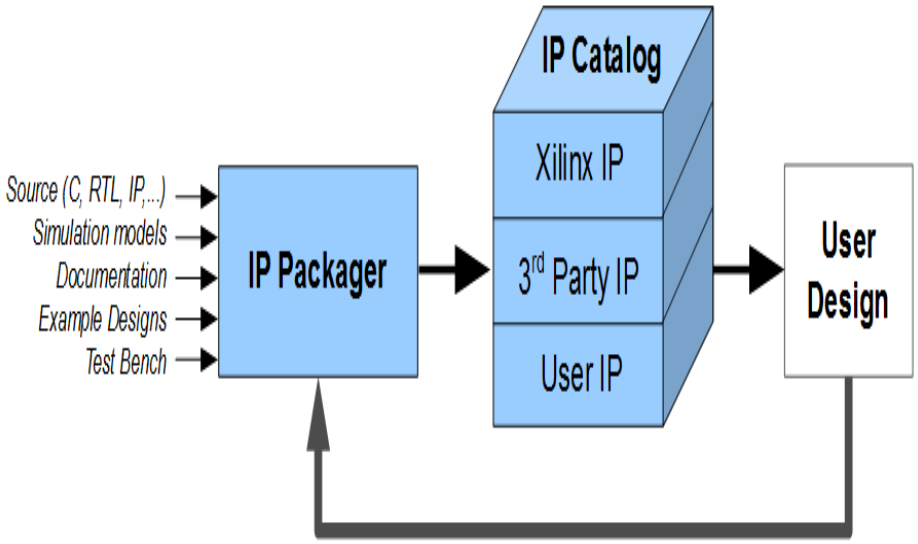

FIG 2.2 VIVADO IP - CENTRIC DESIGN FLOW [8]

To customize IP cores and originate output products, including a Synthesized Design Checkpoint (DCP) use the control IP core Flow. We can design IP cores using source files and information from a project. We can produce IP cores from a defined directory. First generate a template AXI4 peripheral which includes the HDL, drivers, a test application, a Bus Functional Model (BFM), and a sample template. We can use IP cores in either Project or Non-Project modes by intimating the created Xilinx Core Instance (XCI) file, which is a recommended method for huge projects with many team members. Design and add IP cores within a Vivado Project. Access the IP Catalog in a project to create and add IP cores to design. Reserve the IP either inside the project or conserve it externally to the project, which is the endorse method for projects with small team sizes. Construct and customize IP cores and provoke output effects in a non- project script flow, including making of a Synthesized Design Checkpoint (DCP).

5. HARDWARE AND SOFTWARE USED:

The hardware requirement is Zync FPGA[Field Programmable Gate Array].

The software requirement is Xilinx Vivado.

In this we will study Verilog codes for different data path elements like shifters, registers and multipliers.

6. CONCLUSION

Core-based representation is a optimistic way to dole out with the enlarging system model convolution. Utilizing the acquirability of pre-verified cores can considerably fast-track the plan, as only a combination step need to be performed. However, this apparatus often guides to restricted flexibility, mainly if IP's are acquired from third-party dealers, because no prominent of the internal structure is generally allowed, and therefore no internal moderations are achievable. IP's are not generally supplied with the source code and consequently they can only be non-segregated as black packets.

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