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Design and development of Direct Digital Synthesizer on FPGA

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ABSTRACT

This paper explains the analysis of a Direct Digital Synthesizer implemented on FPGA.Using a fixed frequency clock we can generate a continuous waveform in DDS . FPGA board is used to design a DDS because it helps to achieve the user requirements . DDS helps in achieving the requirements of fast frequency and phase switching, signals with high frequency , quality and also high range of tunable frequencies.

Keywords: *DDS, FPGA, LUT, Verilog.*

I. INTRODUCTION

Using DDS we can produce waveforms like sine wave, triangular wave,square wave etc. All the operations in DDS are digital which makes an advantage to achieve change in frequencies more faster and also helps in producing wide range of frequencies. Present generation DDS are designed to operate in low power range.The major requirement for industries is the ability to accurately produce and control waveforms of various frequencies. Here we generating a signal which varies with time in digital form and then performing a digital-to-analog conversion. A designer can generate different frequencies in the range of phase-locked-loop techniques using which we can produce very high range of frequency signals to dynamic programming of digital-to-analog converter which generate arbitrary waveforms at lower frequency. The output frequency that is obtained from a DDS is mainly due to, the clock frequency and the frequency tuning word. Because of its single chip IC, DDS is used in both communication and industrial areas for frequency generation. The major applications of DDS are such as signal generation, function generators, local oscillators, modulators etc. Using high speed serial peripheral-interfaces and with an external clock, DDS are programmed to generate different waves. Frequencies of the range less than 1 Hz to 400 MHz are generated with the help of present DDS devices. Finally the advantages like consuming less power, low cost, its integrated chip and the ability to digitally program and reprogrammability of the output waveform, make DDS devices an efficient solution for the waveform generation.

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II. RELATED WORK

From research on different papers we came to know that DDS have a greater applications in communication system.

2.1 Kenneth A. Essenwanger[1] has stated that "DDSs have been in use since the late 1960s [Gillette, 1969] and have become more and more popular as digital logic has advanced in complexity and performance. Sine output DDSs are not the only type of DDSs [Reinhardt, 1985], but have become the most widely used because of their high spectral purity and all digital implementation."

2.2 Amir M. Sodagar[2] in his paper has stated a different approach for frequency synthesis-" The simplest implementation of parabolic approximation idea is to use the value of phase as the initial guess. This method, which is called "sine- phase difference" technique, saves 2 bits of memory word length [2–5]. Another similar work implementing the above idea is a double trigonometric approximation which has led to a memory word length reduction of 3 bits. The closest initial guess to the target sinusoid is obtained by using parabolic approximation."

III. PROPOSED WORK

From the block diagram it is clear that there are four main modules in DDS. They are phase accumulator, phase to amplitude converter, digital analog converter (DAC) and low pass filter(LPF).Clock plays an important role in output frequency that we obtain and also helps to run the system synchronously. The coding work is done in Verilog HDL language in this paper.

Along with the clock frequency the frequency tuning word also plays an important role in the frequency of the output waveform.

At every rising edge or falling edge of the clock the frequency tuning word(FCW) which is stored in the parallel register is added to the content of data stored in phase accumulator. Initially the content of phase accumulator is zero, once it is added with the FCW the result is stored in it and also sent out for further use. Phase truncation is done before the data is send to LUT i.e phase to amplitude converter, So only a part of the data from the output of phase accumulator is sent as input to the phase to amplitude converter.This reduce the power consumption and complexity of the phase-to-amplitude converter without any damage for the output frequency. The truncated output of the phase accumulator serves as the address to the sine-lookup table where each address in the lookup table is the phase point on the sine wave for a complete cycle of 360 degrees. Thus the look up table contains the amplitude value of wave at each address corresponding to its phase value.

As said before the FCW plays an important role in getting the output signal in two ways like:

1. When the FCW is large, the phase accumulator will take larger jumps in the lookup table and therefore generating high frequency signals.
2. When the FCW is small, the phase accumulator will take smaller jumps in the lookup table and therefore producing low frequency signal.

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The output from the phase to amplitude converter is again truncated to match with the data flow of digital to analogconverter(DAC), which converts the digital data into analog signal. Finally the analog output signal is sent to the low pass filter(LPF) which helps in removing the noise signals generated.

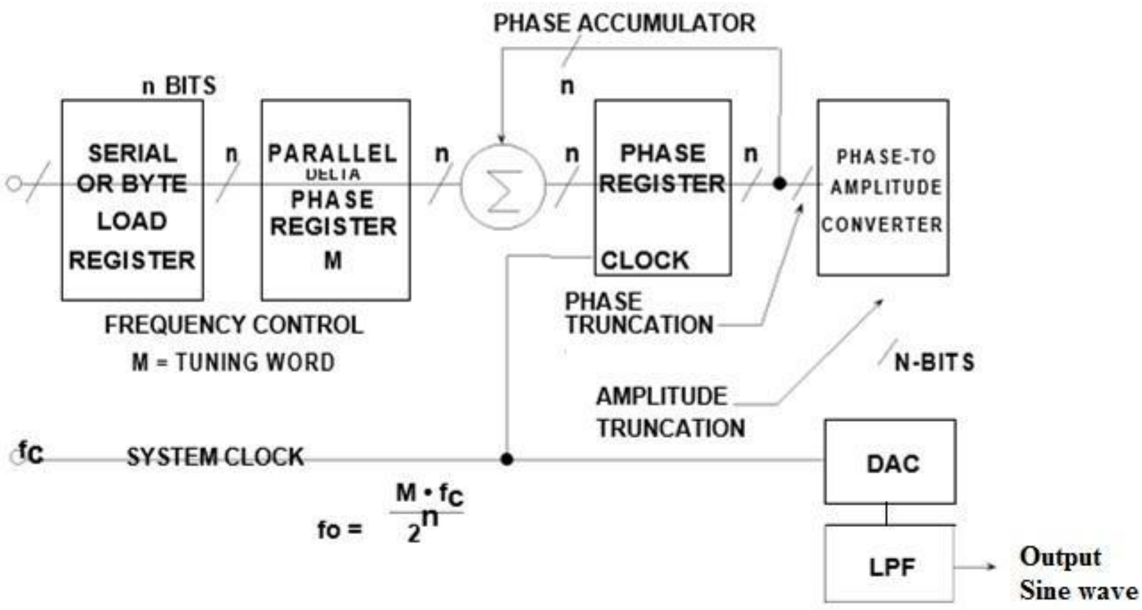

Figure 1: A Flexible DDS System

IV. HARDWARE AND SOFTWARE REQUIREMENTS

Table:4.1

HARDWARE REQUIREMENT	SOFTWARE REQUIREMENT
1. FPGA Board:- Nexys video Artix-7(XC78200T-1SBG484C) 2. Digital to analog convertor:- MAX512CPD 3. Oscilloscope	1. Xilinx VIVADO 2018.3

V. CONCLUSION

The present work shows basic DDS implementation proving the design by synthesis on FPGA. Using this type of model we can generate high frequency signals in range of 100 to 200 MHz with high accuracy and its output frequency, phase and amplitude can be precisely and rapidly manipulated under digital control. Another major

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advantage of this type of model is we can manipulate the code with new ideas which help to improve the performance of the model with same hardware components.

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