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Modelling And Design of Register Banks For MIPS 32 Processor

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ABSTRACT

In view of a legacy manufactured and ceaselessly enhanced over three decades, MIPS engineering is the business' most proficient RISC design, conveying the best execution and least power utilization in a given silicon region .VLSI fashioners can utilize this productivity advantage for noteworthy expense and power reserve funds, or to actualize extra centers to convey an exhibition advantage in a similar power, warm and zone spending plan. MIPS processors are perfect for cutting edge inserted structures over various high-development markets, including advanced purchaser, portable, broadband access and systems administration, best in class interchanges and that's just the beginning.

Keywords : MIPS Processor, Datapath, ALU, register file

I. INTRODUCTION

MIPS design is the business most effective RISC engineering, conveying the best execution and least power utilization in a given silicon area.MIPS is one of the CPU engineering formally upheld by Google's Android, making it perfect for Android-based gadgets, just as a wide scope of different OS including Linux, and a scope of RTOS (constant OS). With billions of MIPS-based items previously transported, and numerous colleges and schools far and wide encouraging CPU design utilizing MIPS as their favored stage.

Introduction to MIPS 32

MIPS 32 is a 32-bit architecture. Registers are 32-bits wide. Arithmetic logical unit (ALU) accepts 32-bit inputs, generates 32- bit outputs . All instruction types are 32-bits long .

MIPS 32 has:

- 32 general-purpose registers (for use by integer operations like subtraction, address calculation, etc)
- 32 floating point registers (for use by floating point addition, multiplication, etc)

II.LITERATURE SURVEY

MIPS is a customary register based RISC design which is generally utilized for showing purposes [1]. Nonetheless, because of it's low unpredictability and effectively extendable guidance set, it is anything but difficult to redo for unique purposes and in this manner it is perfect for execution of explicit applications [2].

There are two ways to deal with executing such a processor, the main methodology being custom VLSI. This methodology is a pricey once-off methodology. The elective methodology is reconfigurable equipment by FPGA (Field Programmable Gate Arrays), which is a lot less expensive. Besides, such a methodology enables the equipment to be effectively adjusted, which permits investigating and alteration even once sent [3].

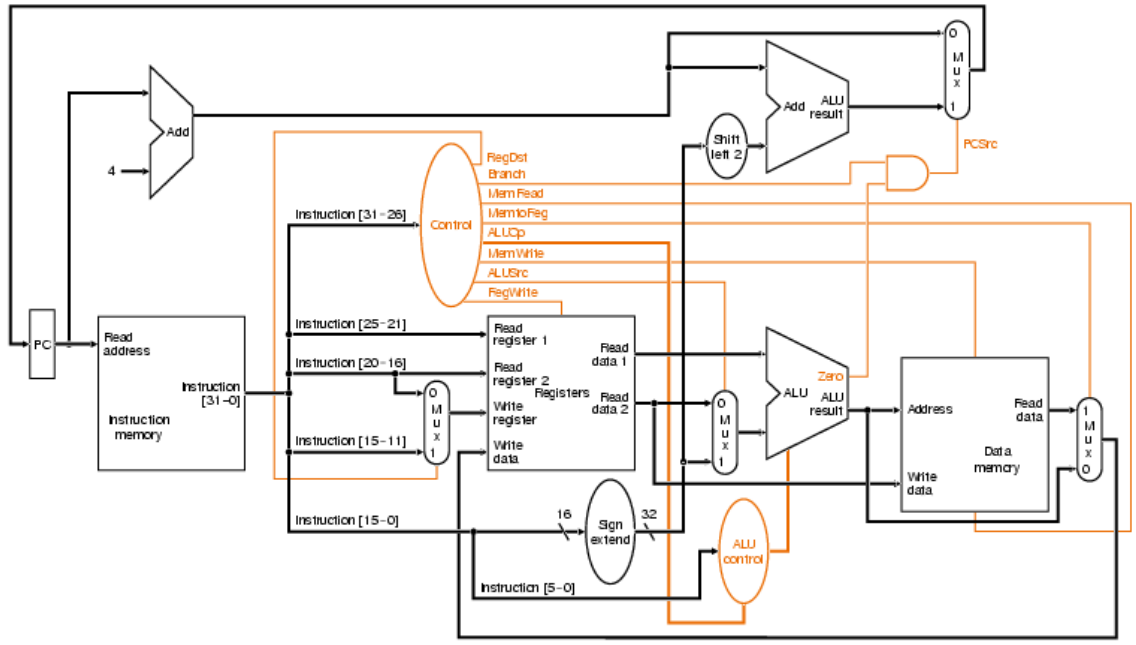
MIPS is an ordinary register based RISC engineering broadly utilized for showing purposes . Because of it's low unpredictability and effectively extendable guidance set, it is anything but difficult to redo for exceptional purposes . There are two ways to deal with executing such a processor, the principal approach being custom VLSI. This methodology is an over the top expensive once-off methodology. The second methodology is reconfigurable equipment by FPGA (Field Programmable Gate Arrays), which is a lot less expensive. such a methodology enables the equipment to be effectively changed, which permits troubleshooting and alteration

even once conveyed.

III. PROPOSED WORK

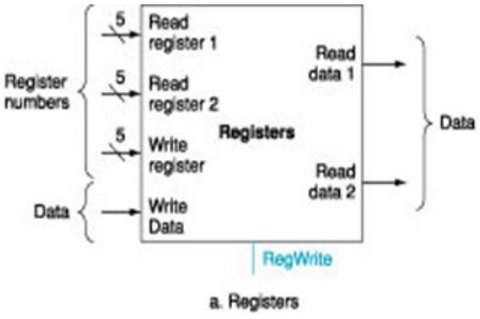
1. Study the MIPS 32 Processor architecture.
2. Develop the Verilog HDL code to design the register bank.
3. Test the developed Verilog code by appropriate test bench and verify the correctness of the system
4. Synthesize the design by using Xilinx Vivado and analyze the power dissipation, area and delay.
5. Finally implement the design by using CADENCE targeted to 180nm technology file. Analyze power dissipation, area and delay.

BLOCK DIAGRAM OF MIPS 32 PROCESSOR:



METHODOLOGY:

Registers in MIPS:



a. Registers

- Designing the register bank, which consist of 32 registers of 32 bits width by using Verilog

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HDL and validating the design by using appropriate test bench.

- In MIPS, there are 32 Registers.
- We need read up to two registers, and write to up to one register.
- Think enlists as D flip-flops. Each register has 32 Dffs.

The control signals are:

- readReg1, readReg2: 5 bits. Used to indicate which reg to peruse.
- Compose Reg: 5-bits. Used to indicate which reg to compose.
- Information: if compose, what information ought to be composed into the reg.
- Reg Write: regardless of whether to compose or not.

IV. HARDWARE AND SOFTWARE REQUIREMENTS

Table:4.1

HARDWARE REQUIREMENT	SOFTWARE REQUIREMENT
1. Zync FPGA processor	**1.** .Xilinx Vivado, CADENCE

VI. CONCLUSION

MIPS processor, which is widely used RISC processor in industry and research area. In this paper, we have successfully designed and synthesized a basic model of Register banks for MIPS 32 processor. The design has been modeled in VHDL and functional verification policies adopted for it. The simulation results shows that area, power and delay of register banks for MIPS 32 processor.

REFERENCES

- Kirat Pal Singh, Shivani Parmar, "Vhdl Implementation of A Mips-32 Pipeline Processor", International Journal of Applied Engineering Research, Vol. 7, pp no.11, 2012.
- Ralph D. Wittig and Paul Chow, "OneChip: An FPGA processor with reconfigurable logic," in Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, Apr. 1996, pp. 126–135.
- Anon. "MIPS Architecture" http://www.cs.wisc.edu/~smoler/x86text/lect.notes/MI PS.html