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Low Power BIST design using Stepped Segment LFSR

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ABSTRACT

Testing of a complex design ensures the reliability of the chip but adds the problem of power dissipation which is a major concern in deep sub-micron technologies. The power dissipation during test mode in a Built-in Self Test (BIST) architecture, which is a widely used Design for Testability (DFT) technique, arises because the consecutive test patterns used have very less correlation increasing the switching activity. In this work, a Stepped Segment Linear Feedback Shift Register (SS-LFSR) is used as a Test Pattern Generator (TPG) to generate test vectors with reduced switching activity. The functionality of the BIST architecture is verified using a combinational circuit of medium complexity as the Circuit under Test (CUT). It is observed that there is a reduction in the power dissipation by about 44% in the BIST architecture using an SS-LFSR as compared to one of the existing test generation methodologies with a slight reduction in the fault coverage.

Keywords *- BIST, DFT, Dynamic power optimization, Fault coverage, LFSR.*

1. INTRODUCTION

As the system complexity is increasing with every passing day, the power dissipation in the highly dense system is on the rise. The power dissipation in the system can be classified as dynamic power and static power. The static power is negligible when compared to the dynamic power dissipation; hence we consider strategies to optimize the dynamic power dissipation in the system. The dynamic power can be mathematically represented as: $P_d = \alpha\ V_{dd}^2\ f\ C_L$ (1). From the equation, it is clear that the power dissipation depends on the switching activity (α), the supply voltage (V_{dd}), the frequency of operation (f) and the parasitic capacitance (C_L). In this work a reduction in the power dissipation in complex VLSI systems is achieved by reducing the switching activity.

Highly complex VLSI systems need to undergo testing to ensure reliability. BIST is one of the most widely preferred DFT approach. When we consider the BIST architecture, the major source of power dissipation arises from the LFSR block (used as a TPG) as the test patterns generated tend to be random with a relatively higher rate of switching activity and hence a number of approaches to optimize the LFSR have been devised. Some of the approaches are Modified Clock LFSR (MC-LFSR) [1], Bit Swapping LFSR (BS-LFSR) [2], Bit Swapping with Modified Clock LFSR (BS-MC LFSR) [3] etc. Stepped Segment LFSR (SS-LFSR) [4] is another approach to reduce the transitions between the test vectors and is achieved by segmenting the conventional LFSR into segments. Each of the segments is controlled by a separate clock generated such that at any time only one segment is activated alternatively while the rest of the segments remain non-operational. Segmentation of the

flip-flops ensures that the number of transitions between test vectors reduces, decreasing the switching activity which eventually reduces the power dissipation during testing. In this paper, two approaches to optimize the LFSR block are taken up and the performance of the BIST architecture using each of the LFSR blocks is compared in terms of power, fault coverage and area overhead.

2. BIST ARCHITECTURE

The basic BIST architecture [5] consists of a Test Pattern Generator (TPG), an output response analyzer and a test controller as the major hardware blocks as shown in Fig 1.

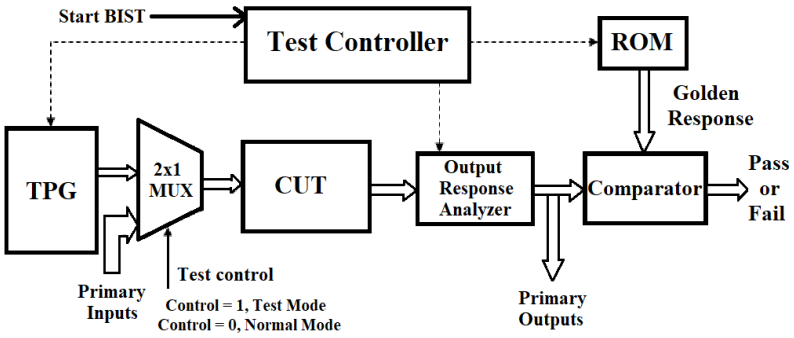

Figure 1: Basic BIST architecture

An LFSR, a widely used TPG in the BIST architecture generates the test vectors required. The signature analyzer is the preferred compaction technique used in BIST for the output response analysis. The test controller initiates and controls all BIST operation. The patterns generated by the TPG are applied to the CUT and the outputs obtained are compacted using signature analyzer and the signature is computed. The computed signature is compared with the golden response (fault-free response) stored in the ROM. If there is a mismatch, it indicates the presence of fault in the CUT.

Since the LFSR block in the BIST architecture contributes to the major portion of the power dissipation, various approaches have been modeled to optimize the LFSR block. The coming section discusses about the BS-LFSR and the SS-LFSR and how the SS-LFSR reduces the power dissipation in the BIST architecture when compared to the BS-LFSR.

3. BIT SWAPPING LFSR (BS-LFSR)

The BS-LFSR, like a conventional LFSR generates random patterns by adding exclusive-OR gates on the outputs of two or more flip – flops to obtain the feedback and providing the feedback to the input of the flip – flop. Extra 2 x 1 multiplexers are employed to enable the bit swapping operation and reduce the transitions.

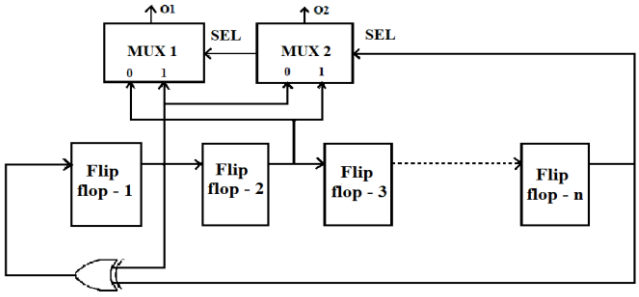

Figure 2: n-bit BS-LFSR

For the n-bit BS-LFSR shown in Fig 2, one of the outputs is considered as the select line for the multiplexers (usually the nth bit is chosen as the select line). When n is odd and bit n = 0, bit 1 will be swapped with bit 2, bit 3 with bit 4, and bit n-2 with bit n-1. If n is even and bit n = 0, bit 1 will be swapped with bit 2, bit 3 with bit 4, and bit n-3 with bit n-2. In all cases of the selection line, bit n is excluded from the swapping operation. When bit n = 1, no swapping will be performed.

4. STEPPED SEGMENT LFSR (SS-LFSR)

The SS-LFSR generates patterns by dividing the conventional LFSR into segments with two or more flip-flops in each segment. Each segment is then controlled by a separate clock generated by the clock generation unit shown in Fig 4. A 4-bit SS-LFSR as shown in Fig 3 consists of two segments with two flip-flops in each segment. The two segments are separated by a dummy flip-flop (loaded with an initial value at the start of the operation) which stores the value of the last flip-flop in the previous segment after every clock cycle. Each of the segments is controlled by clocks seg_clk1 and seg_clk2 which ensure that either segment 1 or segment 2 is active at any time. The number of transitions between successive test patterns is limited to the number of flip-flops in each segment; hence a reduction in the number of transitions is attained.

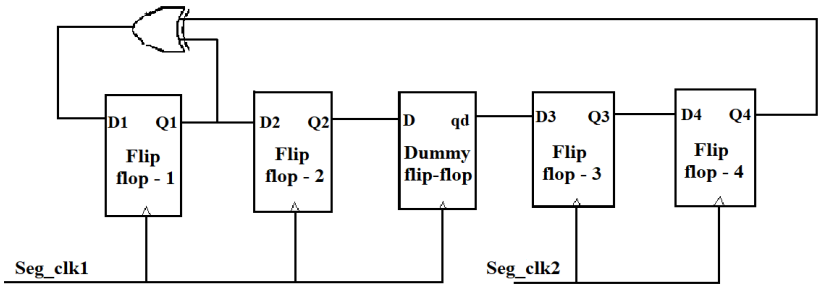

Figure 3: 4-bit SS-LFSR

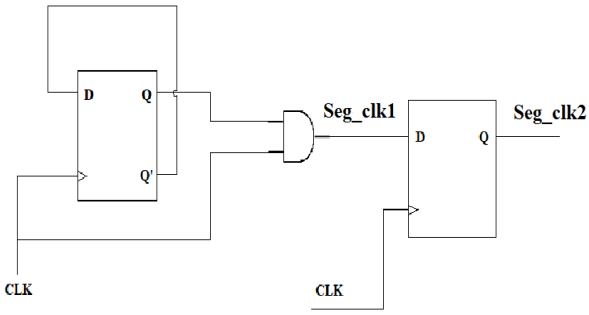

Figure 4: Clock generation unit

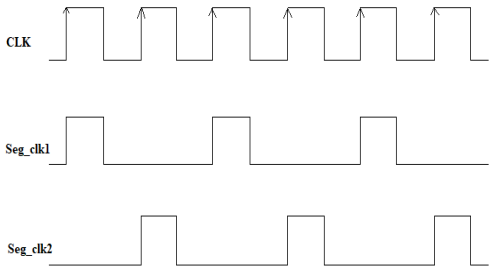

Figure 5: Generated Clock waveform

The above BIST architecture is modeled using Verilog HDL. The simulation and synthesis are carried out using Vivado HLS. The CUT used here is a conventional 3x3 array multiplier. Patterns are applied from a 6-bit BS-LFSR and a 6-bit SS-LFSR to the array multiplier. An MISR is used for compaction and the computed signature is compared with the golden response stored in the ROM to determine whether the circuit is faulty or fault-free. A comparison is carried out between the BIST architecture using the BS-LFSR and the SS-LFSR in terms of power, fault coverage and area overhead.

5. RESULTS AND DISCUSSION

5.1 POWER ANALYSIS

The power reports for the BIST architecture using a 6-bit BS-LFSR shown in the Fig 6 indicate that the total on-chip power is 6.63W and for SS-LFSR case as the TPG is 3.71W as shown in Fig 7. There is a reduction in power by about 44% in the BIST architecture using the SS-LFSR compared to the BS-LFSR case due to the reduction in the number of transitions between test patterns.

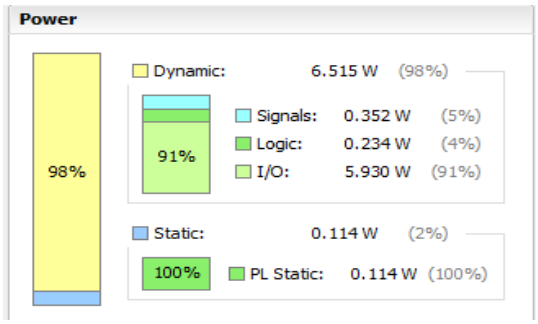

Figure 6: Power dissipation in the BIST architecture using 6-bit BS-LFSR

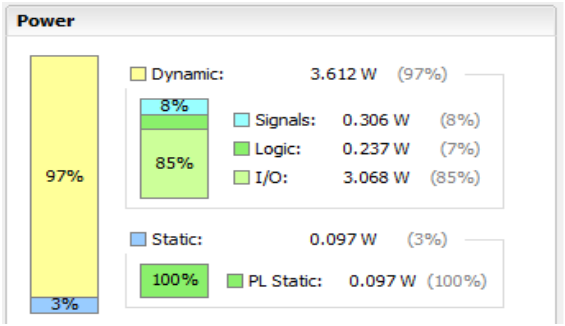

Figure 7: Power dissipation in the BIST architecture using 6-bit SS-LFSR.

5.2 FAULT COVERAGE

Fault coverage is defined as the percentage of faults that can be detected during a certain test procedure. In this work, all single stuck-at-faults of the CUT are exhaustively tested for twenty clock cycles. The fault coverage for

the BIST architecture employing the SS-LFSR is 96% and for the BS-LFSR case is 98%. The decrease in the fault coverage for BIST architecture using the SS-LFSR is due to repeated test patterns generated by the SS-LFSR whereas, the BS-LFSR generates completely random test patterns.

5.3 DEVICE UTILISATION

The reports shown in Fig 8 and Fig 9 obtained post implementation in the Vivado HLS simulator indicate that there is a slight increase in the area overhead for the BIST architecture using the SS-LFSR when compared to the BIST using the BS-LFSR. The increase in the area overhead in the SS-LFSR case arises due to the additional circuitry that is used for the clock generation to enable the stepped segment activation of the flip-flops.

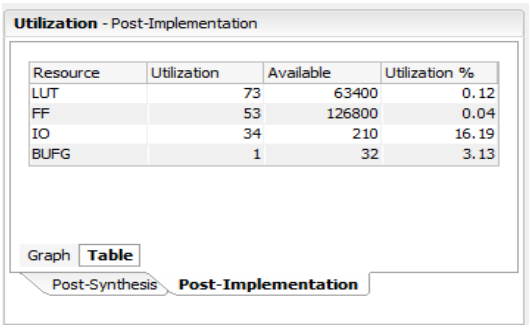

Figure 8: Utilization reports of BIST architecture using 6-bit SS-LFSR

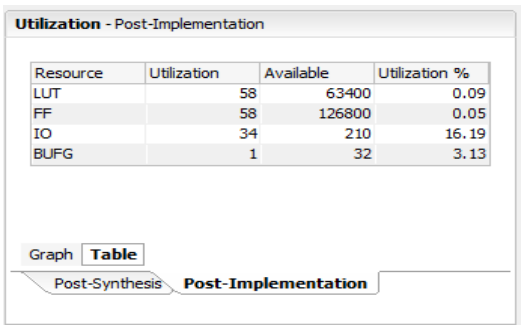

Figure 9: Utilization reports of BIST architecture using 6-bit BS-LFSR

A comparison between the BIST architectures using the BS-LFSR and the SS-LFSR is tabulated in Table 1.

Table 1: Comparison of test power, fault coverage and device utilization.

LFSR	BIST using 6-bit BS-LFSR	BIST using 6-bit SS-LFSR
Test cycles	20	20
Test Power	6.63W	3.71W
Fault Coverage	98%	96%
Device utilization (Number of LUTs)	58	73

As the number of segments of the SS-LFSR increases, the power dissipation gradually decreases. If we consider the case of an 8-bit SS-LFSR, the 8-bit SS-LFSR with four segments with two flip-flops in each

segment (a dummy flip-flop separates each of the segments) has a total on-chip power of 4.9W as shown in Fig 10, whereas the SS-LFSR with two segments (four flip-flops in each segment) has a total on-chip power of 7.9W as shown in Fig 11.

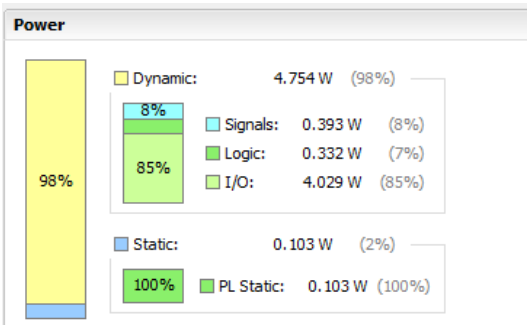

Figure 10: Power dissipation in BIST using 8-bit SS-LFSR with four segments.

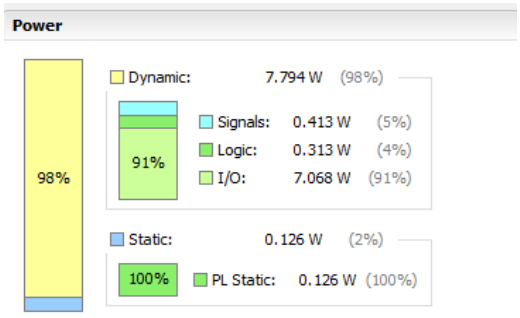

Figure 11: Power dissipation in BIST using 8-bit SS-LFSR with two segments

A power reduction of about 38% is achieved for the BIST architecture employing an 8-bit SS-LFSR with four segments when compared to the BIST architecture employing an 8-bit LFSR with two segments due to the decrease in the number of transitions in the former case. The SS-LFSR with four segments has a maximum of two transitions between successive patterns, whereas for the SS-LFSR with two segments, the maximum number of transitions between any two patterns is four, hence lesser transitions for the former case. Hence low power designs can be achieved when the LFSR design consists of more segments.

6. CONCLUSIONS

From the above discussion, it can be concluded that the BIST architecture using 6-bit SS-LFSR provides a reduction in the power dissipation when compared to the BIST architecture using 6-bit BS-LFSR by about 44%. The fault coverage for the BIST architecture using the SS-LFSR is reduced by 2% compared to the BIST architecture using the BS-LFSR; whereas there is an additional area overhead for the SS-LFSR case compared to the BS-LFSR case due to the additional clock generation circuitry that is to be used for stepped segment activation of the flip-flops. Therefore, a reduction in power dissipation in the SS-LFSR case is achieved at the expense of reduced fault coverage and increased area overhead compared to the BS-LFSR case. Also, as the number of segments increases, the power dissipation decreases. For the BIST architecture using an 8-bit SS-LFSR, the SS-LFSR having four segments results in a power reduction by 38% when compared to the SS-LFSR with two segments.

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