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DEVELOPMENT OF WIND ENERGY CONVERSION SYSTEM USING MULTIPULSE DFIG

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ABSTRACT

Wind Energy is one of the favorable renewable energy resources and the multilevel inverter has been proven to be one of the important enabling technologies in wind energy conversion system (WECS) utilization. Wind energy conversion system with utilization grid systems are getting more and more widespread with the increase in the energy demand and the concern for the environmental pollution around the world. With multilevel inverters harmonic content gets reduced and with more levels the output approaches the sine wave. The voltage stress also gets reduced. In this paper we are trying to implement a WECS with Multilevel voltage source inverters using SPWM. The need of several sources on the DC side of the converter makes multilevel technology attractive for WECS applications. This paper analyzes the structure of an 84-pulse voltage source converter (VSC), assembled by combining one twelve-pulse VSC, in conjunction with an asymmetric single phase seven-level converter plus an injection transformer. It restricts the compensating voltages during the sag whenever it predicts that a maximum limit for the flux linkage is about to be exceeded. The prediction is carried out at the beginning of a stabilized voltage sag. Moreover, the technique allows a certain level of sag compensation even when the estimated flux is expected to exceed the saturation limit. The proposed strategy allows savings in the number of employed switches. Simulations results are provided to show the proposal appropriateness.

Key words: Doubly fed induction generator (DFIG), Power leveling, sensor less, Six-pulse generator, Seven level converter, wind energy conversion system (WECS).

I.INTRODUCTION

In response to the new grid code requirements, several DFIG models have been suggested recently [8], including the full-model which is a 5th order model. These models use quadrature and direct components of rotor voltage in an appropriate reference frame to provide fast regulation of voltage. The 3rd order model of DFIG which uses a rotor current, not a rotor voltage as control parameter can also be applied to provide very fast regulation of instantaneous currents with the penalty of losing accuracy. Apart from that, the 3rd order model can be achieved by neglecting the rate of change of stator flux linkage (transient stability model), given rotor voltage as control parameter. Additionally, in order to model back-to back PWM converters [7], in the

simplest scenario, it is assumed that the converters are ideal and the DC-link voltage between the converters is constant. Consequently, depending on the converter control, a controllable voltage (current) source can be implemented to represent the operation of the rotor-side of the converter in the model. However, in reality DC-link voltage does not keep constant but starts increasing during fault condition. Therefore, based on the above assumption it would not be possible to determine whether or not the DFIG will actually trip following a fault. Power Quality problems encompass a wide range of disturbances such as voltage sags/swells, flicker, harmonics distortion, impulse transient, and interruptions [9][10]. Voltage sags can occur at any instant of time, with amplitudes ranging from 10 – 90% and a duration lasting for half a cycle to one minute**.** Voltage swell, on the other hand, is defined as a swell is defined as an increase in RMS voltage or current at the power frequency for durations from 0.5 cycles to 1 min. typical magnitudes are between 1.1 and 1.8 up. Swell magnitude is also is also described by its remaining voltage, in this case, always greater than 1.0.Voltage swells are not as important as voltage sags because they are less common in distribution systems[6].

Voltage sag and swell can cause sensitive equipment (such as found in semiconductor or chemical plants) to fail, or shutdown, as well as create a large current unbalance that could blow fuses or trip breakers. These effects can be very expensive for the customer, ranging from minor quality variations to production downtime and equipment damage. There are many different methods to mitigate voltage sags and swells, but the use of a custom Power device is considered to be the most efficient method. Switching off a large inductive load or Energizing a large capacitor bank is a typical system event that causes swells[2]. This paper introduces DFIG and its operating principle. Then, a simple control based on dqo method is used to compensate voltage sags/swell. At the end, MATLAB/SIMULINK model [11] based simulated results were presented to validate the effectiveness of the proposed control method of DFIG. The output results are shown in Fig.(4).

II.CONVENTIONAL SYSTEM CONFIGURATION OF DFIG

Dynamic Voltage Restorer is a series connected device designed to maintain a constant RMS
Voltage value across a sensitive load. The DFIG considered consists of:

a. An injection / series transformer
b. A harmonic filter,
c. A Voltage Source Converter (VSC),
d. An energy storage and
e. A control system

III.SIX-PULSE GENERATOR

The second block is the six-pulse generator, responsible for generating the pulse sequence to fire the three-phase IGBT array. It consists of an array of six-pulse spaced 60° each other. The IGBT will operate at full 180° for the *on* period and 180° for the *off* period[3]. Any disturbance on the frequency will be captured by the

synchronizing block, preventing malfunctioning. The falling border in the synchronizing block output signal is added to a series of six 60° spaced signals.

The modulus operator with the 2π argument gives the needed *on* sequence that will be sent to the gate opto-coupler block, which will feed each six-pulse converter. The *off* sequence

turns out on a similar way but waiting 180° to keep the same *on* and *off* duration in each IGBT.

IV.SEVEN-LEVEL PULSE GENERATOR

To operate the seven-level inverter, six times the frequency of the six-pulse generator must be ensured. This is achieved by monitoring the falling border in the novel PLL output signal, using it along with the modulus operator with the π/3 argument. This signal will be the period for the seven-level generator which will change its state each π/42 rad and the output of seven level pulse generator is shown in Fig.(2).

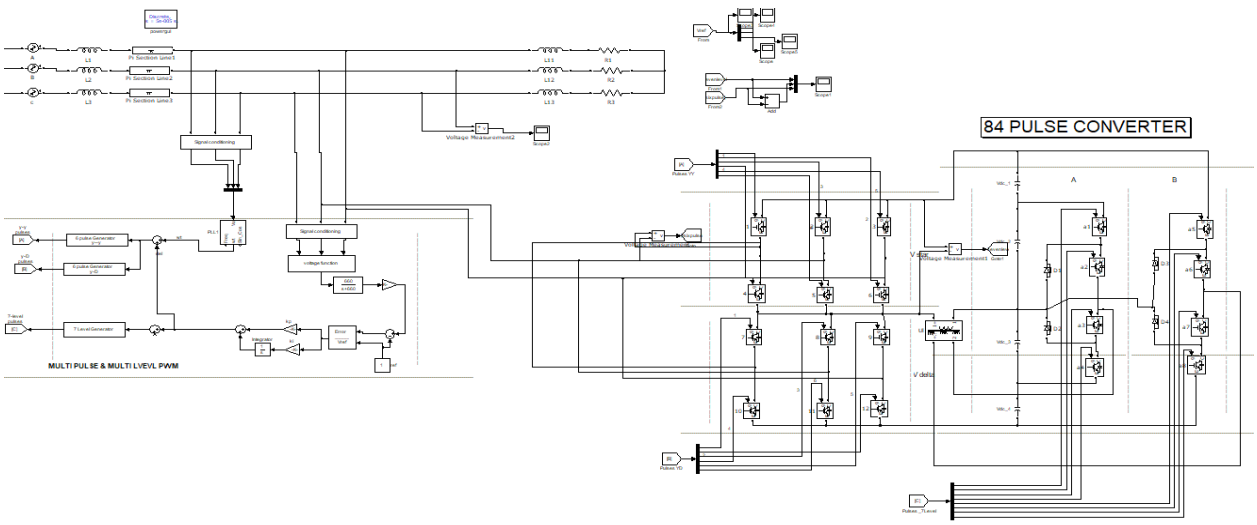

Fig.1 Simulation of 84 pulse DFIG

$$V_U(t) = \sum_{n=1}^{\infty} V_{U_{2n-1}} \sin\left((2n-1)\omega t\right)$$

$$V_{U_{2n-1}} = \frac{4V}{3\pi(2n-1)}\left(A_{2n-1} + aB_{2n-1}\right)$$

$$A_{2n-1} = 2 + 2\cos\left(\frac{1}{3}\pi(2n-1)\right) + 2\sqrt{3}\cos\left(\frac{1}{6}\pi(2n-1)\right)$$

$$B_{2n-1} = \sum_{i=0}^{20} Coeff_i \cos\left(\frac{i}{42}\pi(2n-1)\right)$$

where

$$Coeff = \begin{Bmatrix} -3, & 1, & 1, & 1, & 1, & 1, & 1,\ldots \\ -3\sqrt{3}, & \sqrt{3}-1, & \sqrt{3}-1, & \sqrt{3}-1, & \sqrt{3}-1, & \sqrt{3}-1, & \sqrt{3}-1,\ldots \\ -3, & -\sqrt{3}+2, & -\sqrt{3}+2, & -\sqrt{3}+2, & -\sqrt{3}+2, & -\sqrt{3}+2, & -\sqrt{3}+2 \end{Bmatrix}$$

A single-phase structure of an m-level cascaded inverter[4] is illustrated in Fig(1). Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Fig(1). The phase voltage v_{an} = $v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$.

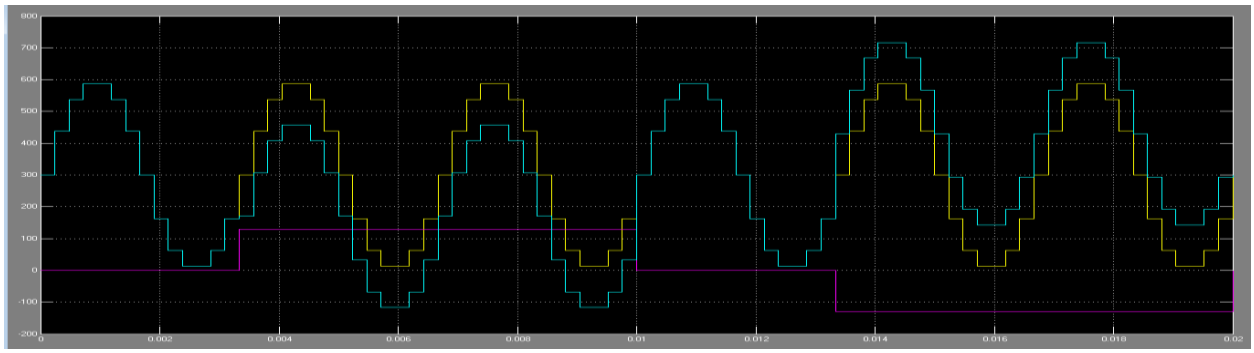

Fig.2. Mixing seven-level, six-pulse signals, and transformer's ratios to attain V_{an} and $V_{\Delta U}$.

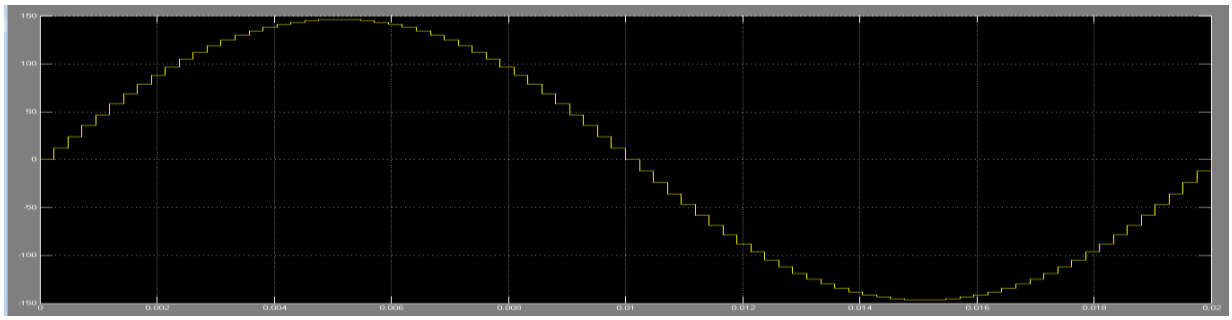

Fig.3. 84-pulse line-to-neutral output voltage

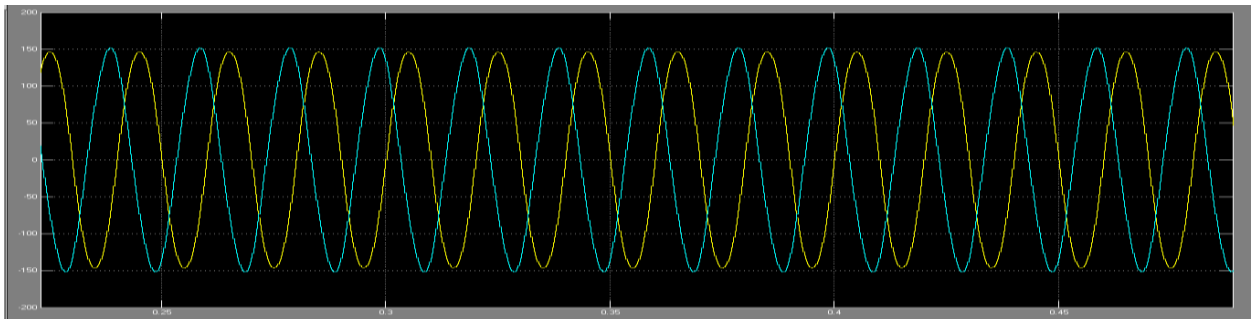

Fig.4 . Phase voltages after compensation

The 84-pulse signal value (*VU*) depends on the injection transformer turns ratio *a*, which is determined so as to minimize the total harmonic distortion (THD)[5], The output of 84 pulses is shown in Fig.(3)

$$THD_{VU} = \sqrt{\frac{\sum_{n=2}^{\infty} V_{Un}^2}{V_{U1}^2}}$$

The minimization of THD yields the parameter *a*. In this paper such estimation has been made through MATLAB for a value $n = 7200$, with increments of $a = 0.0001$. With these parameters, the minimum THD becomes 2.36% which is shown in Fig.(5)with $a = 0.5609$, value employed in previous figures. According to the IEEE Std. 519, the distortion limits indicate that the allowed THD voltage is 10% in dedicated systems, 5% in general systems, and 3% for special applications as hospitals and airports. Through our proposition, the resultant THD allows its use even in applications with stringent quality requirements, it exhibits less dependence to variations in the transformer's turn ratio *a*, which can have a variation until $\pm$12.5%to reach a maximum THD lower than 3%. This means that it does not need a strict reinjection transformer turn ratio in order to get the THD for stringent conditions.

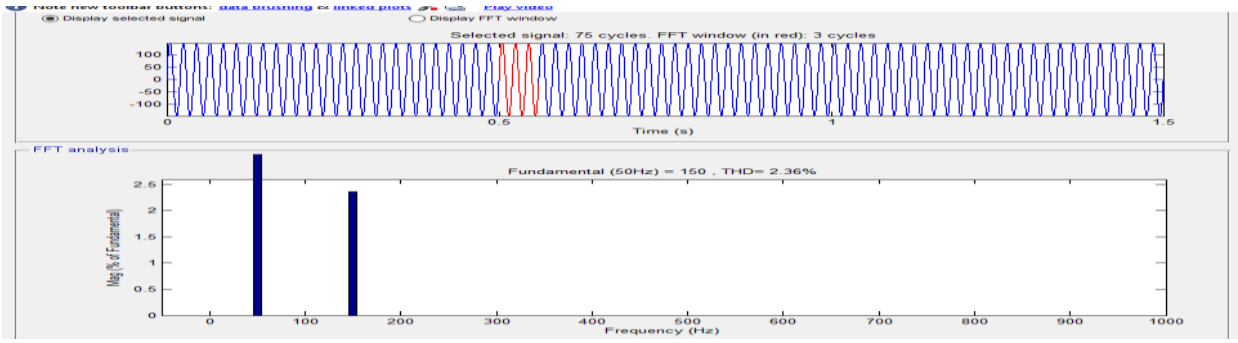

Fig. 5. THD analysis of proposed 84 pulse converter (THD 2.36%)

V.CONCLUSION

The modeling and simulation of a DFIG using MATLAB/SIMULINK has been presented. A control system based on dqo technique which is a scaled error of the between source side of the DFIG and its reference for sags/swell correction has been presented. The simulation shows that the DFIG performance is satisfactory in mitigating voltage sags/swells. This paper describes the strategy to obtain an 84-pulse VSC three-phase voltage with the associated low THD, by combining one twelve-pulse converter plus a seven-level converter. The device performance, proven on a lab prototype, allows to verify the harmonic content of the resultant voltage signal. The exhibited low THD, permits the system to be used in especial application devices. The three-phase digital PLL used to detect the phase of the fundamental voltage, synchronizes the firing signals in all switches within a sample cycle.

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