

DESIGN AND IMPLEMENTATION OF DELAY AND POWER EFFICIENT MULTIPLIER

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ABSTRACT

Multiplication is the most basic and frequently used operations in a digital computer. With advances in technology, various techniques have been proposed to design multipliers, which offer high speed, low power consumption and lesser area. These three parameters i.e. power, area and speed are important parameters for VLSI system.. In this paper Vedic Mathematics is used to implement the algorithm of multiplication. Vedic Mathematics is based on 16 formulas with the purpose of simplification of lengthy and cumbersome mathematics. Vedic mathematics contains multiple algorithms for one operation. In the current work the multiplication algorithms are evaluated for their suitability in binary arithmetic. It has been found that Urdhva tiryakbhyam Sutra is most efficient Sutra (Algorithm), giving minimum delay & power consumption for multiplication of all types of numbers, either small or large. This algorithm is implemented for Multiplication in VHDL by Xilinx Synthesis Tool ISE 8.1. Further, the Vedic multiplier (8x8) results are compared with Array, Wallace tree & Dadda multipliers.

Keywords: Dadda, Urdhava Triyakbhyam sutra, Vedic multiplier, VHDL, VLSI, Wallace Tree.

1. INTRODUCTION

A central processing unit devotes a considerable amount of processing time in performing arithmetic operations, particularly multiplication operations. Multiplication is one of the basic arithmetic operations and it requires substantially more hardware resources and processing time than addition and subtraction. Digital signal processing (DSP) is the technology that is present in almost every engineering discipline. It is also the fastest growing technology of this century and, therefore, it poses tremendous challenges to the engineering community. Faster additions and multiplications are of extreme importance in DSP for convolution, discrete Fourier transforms, Fast Fourier Transforms and digital filters. Due to the importance of digital multipliers in DSP, it has always been an active area of research and a number of interesting multiplication algorithms have

been reported in the literature. This work presents a systematic design methodology for fast and area efficient digit multiplier based on Vedic mathematics. The Multiplier Architecture is based on the Vertical and Crosswise algorithm of ancient Indian Vedic Mathematics [1]. A lot of work has been done in this field. But still many aspects are not touched. S, Akhter in 2007 presented a novel technique for digital multiplication that is quite different from the conventional method of multiplication like add and shift [1]. M. Pradhan et.al in 2011 investigated the concepts behind the “Urdhava triyakbhayam sutra” and “Nikhilam sutra” of multiplication [2]. H. Durga Tiwari, et.al in 2008 proposed a new multiplier & square architecture based upon Vedic mathematics for low power and high speed applications. It is based on generating all partial products and their sum in one step. This paper concludes that Urdhva triyakbhayam, being general mathematical formula, is equally applicable to all cases of multiplication. D. Jaina, et.al in 2011 proposed a MAC unit having a multiplier based upon “Urdhava Triyakbhayam sutra”. The proposed Vedic mathematics based MAC unit is highly efficient in terms of speed. It has regular and parallel structure [5]. Y. Bansal et.al proposed a 16 bit Vedic multiplier with 'Urdhava-triyakbhayam' methodology using compressor adders. Compressor adders add more than 4 bits at a time and use multiplexers in its circuitry which reduces the XOR gate operation and this results in reduction in delay [11].

This Paper is structured as Follows: Section 1 introduce the related work regarding Vedic multipliers. Section 2 briefly introduce Urdhava Triyakbhayam sutra. Section 3 represents the Schematics of Vedic multiplier designed using urdhava Triyakbhayam sutra and their waveforms. Section 4 shows the simulation results of device utilization, Power Dissipation and Delay of these designs. Section 5 includes the future work. Finally Section 6 comprises of conclusion.

2. URDHAVA TRIYAKBHYAM SUTRA

The multiplier is based on an algorithm Urdhva Triyakbhayam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Triyakbhayam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means “Vertically and crosswise”. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using Urdhava Triyakbhayam explained in fig 1. The algorithm can be generalized for $n \times n$ bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip.

The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of silicon area/speed [9, 10].

2.1. Multiplication of two decimal numbers- 225*316

To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (225 * 316). The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero.

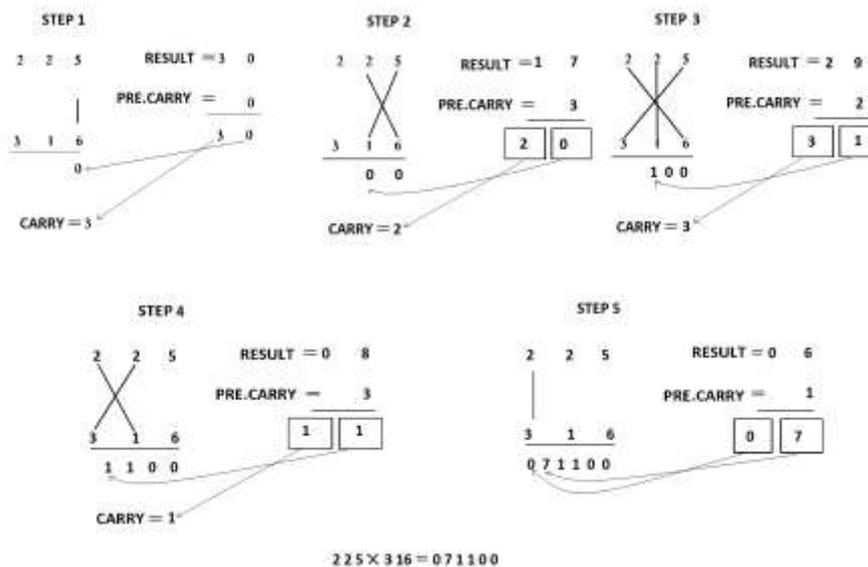


Fig.1 Multiplication of two decimal numbers by Urdhva Tiryakbhyam

2.2 Algorithm for N x N bit Vedic multiplier Using Urdhva Tiryakbhyam (Vertically and crosswise) for two Binary numbers:

For NxN multiplication, divide the multiplicand and multiplier into two parts, consisting of (N to N/2-1) bits and (N/2 to 1) bits. For example, for multiplication of A and B, of 16 bit each, if A=0000001010101101, then its part will be 00000010, and 10101101. Similarly divided B is equal parts, i.e. if B= 0010001110101011, then its part will be 00100011 and 10101011. Represent the above mentioned parts of A as Am and Al. Similarly for the B, it is Bm and Bl. Now represent A and B as AmAl and BmBl. For A X B, we can have

$$\begin{matrix} A_m A_l \\ B_m B_l \\ \hline \end{matrix}$$

$$\begin{array}{ccc}
 A_m \times B_m & A_m \times B_l & A_l \times B_l \\
 & & A_l \times B_m
 \end{array}$$

Fig. 2 General Representation for Vedic multiplication

The individual multiplications product can be obtained by the same partitioning method discussed earlier. In the above example, we have to use 8 bit multiplier for each product term. Let's say, the overall result is to be represented in $S_{31} \dots S_0$. Now for each of the above multiplication, output will be sampled in 8 bit each. For the product $A_m \times B_m$, use $S_{15} \dots S_0$. Similarly for the rest of the product term use $S_{31} \dots S_{16}$, $S_{15} \dots S_0$, $S_{31} \dots S_{16}$, $S_{15} \dots S_0$. Now the whole pattern of output from the 8 bit multiplier will look like $S_{15} \dots S_0 \ S_{31} \dots S_{16} \ S_{15} \dots S_0 \ S_{31} \dots S_{16} \ S_{15} \dots S_0$. [1]

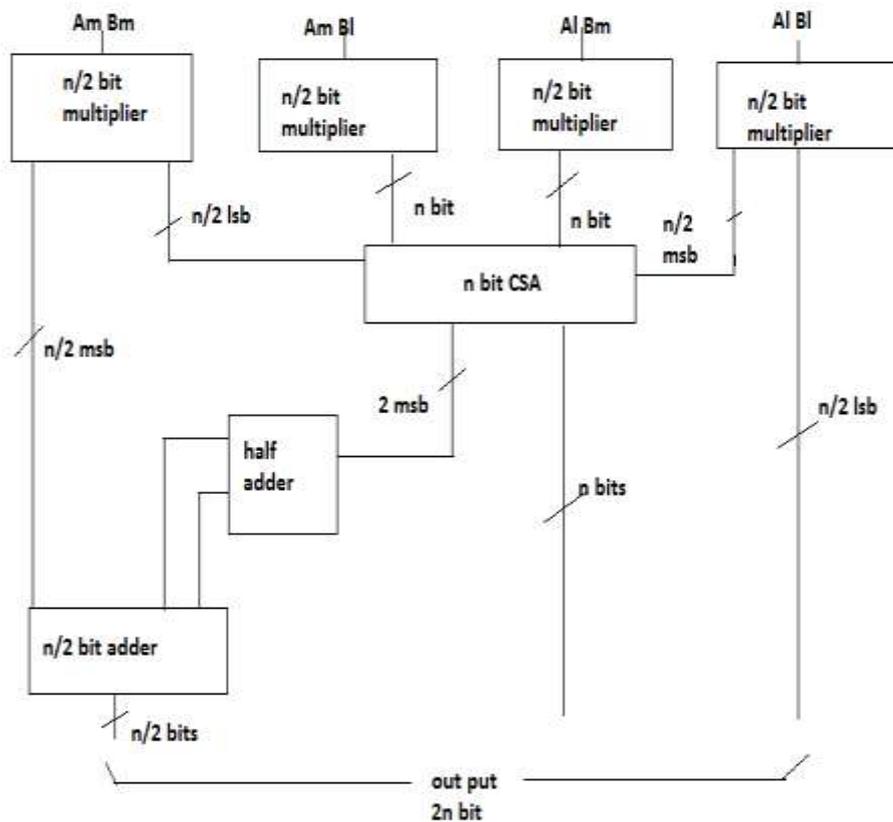


Fig. 3 Complete block diagram for n x n bit vedic multiplier architecture

Fig. 3 shows the $n \times n$ bit multiplier architecture based upon vedic algorithm Urdhava triyakbhyam. For $n \times n$ bit multiplication four $n/2 \times n/2$ multipliers are required. To add the partial products n bit carry save adder, one half adder & one $n/2$ bit full adder is required.

3. VEDIC MULTIPLIER REALIZATION

3.1 8X8 BIT VEDIC MULTIPLIER

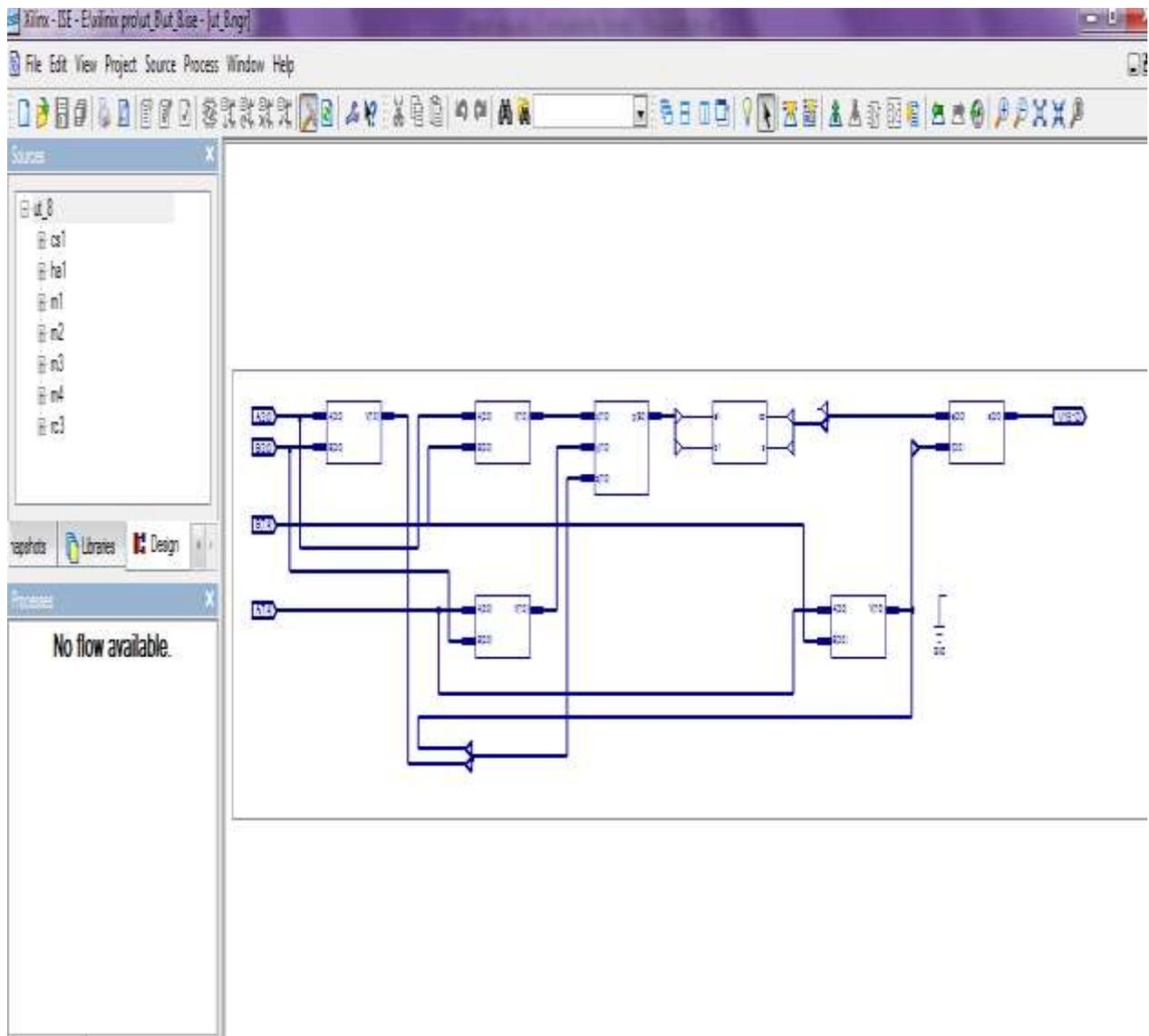


Fig.4 8x8 bit vedic multiplier

3.2 8X8 BIT VEDIC MULTIPLIER WAVEFORMS

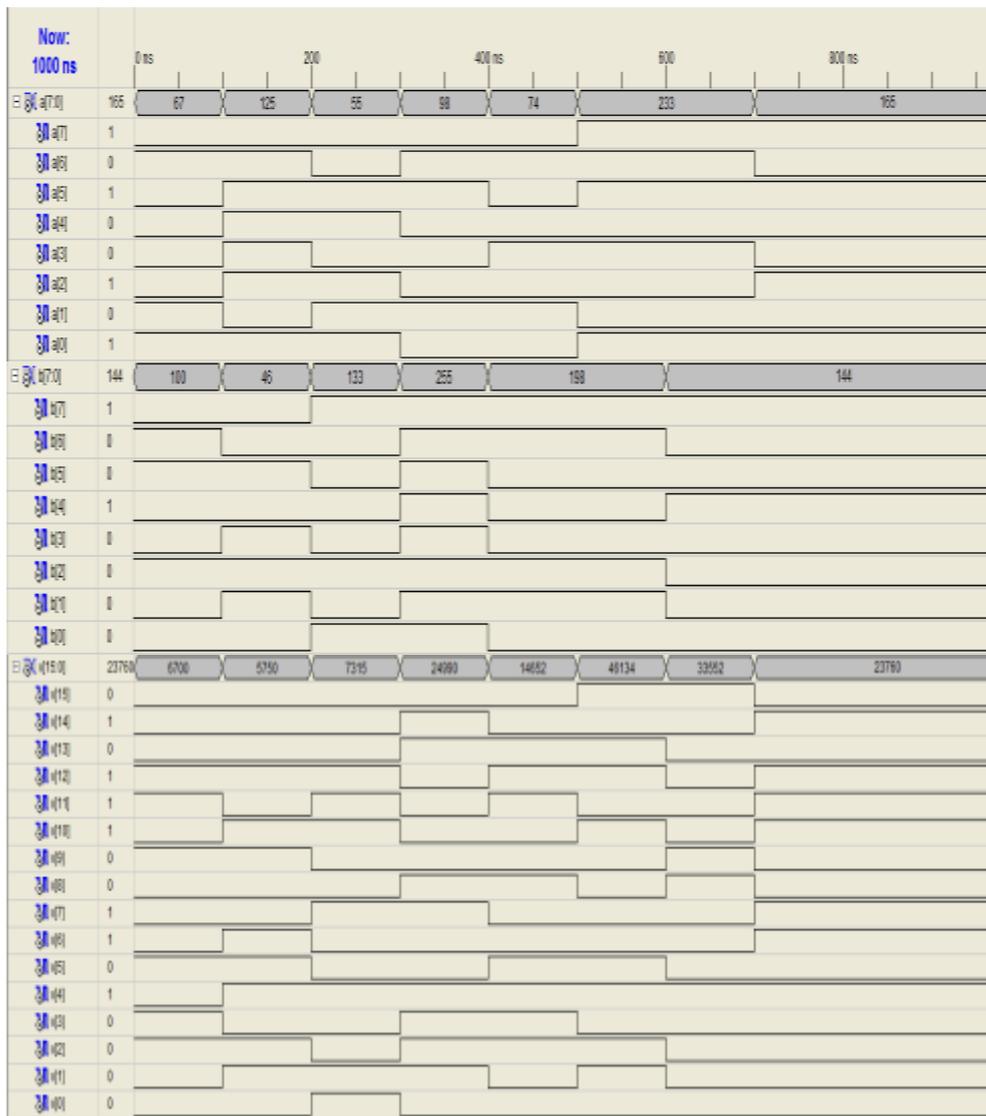


Fig. 5 Simulation Waveform of 8x8 bit Vedic multiplier

4. SIMULATION RESULTS

The Performance of the proposed multiplier is evaluated based on their Area, Power dissipation, Delay. All the simulations are performed using Xilinx ISE 8.1i. Power dissipation of the multipliers is measured using Xpower tool at different frequencies & supply voltages as mentioned in Table I.

Table I shows the simulation results for 8x8 bit multiplier Performance comparison, regarding area, power dissipation and Propagation delay. All the multipliers were supplied with different voltages (2V, 1.2V and 1.8V) and the maximum frequency for the inputs was 20 Mhz and 50MHz.

TABLE-I

Simulation Results of 8x8 Bit Multipliers

Device Spartan 2xc2s100:- 5tq144	Array Multiplier	Wallace Tree Multiplier	Dadda Multiplier	Vedic Multiplier
No. Of Slices	70	90	83	84
No. Of 4 Input LUTs	121	157	145	146
No. Of Bonded IOBs	32	33	32	32
DELAY(ns)	37.153	39.156	36.993	35.440
Power Dissipation (Mw)AT (20 Mhz 2v)	43	37	44	30
AT (20MHZ,1.8V)	37	31	38	25
AT (20MHZ 1.2V)	21	18	22	15
AT (50HZ,2V)	90	76	84	64
AT (50MHZ,1.8V)	75	63	70	53
AT (50MHZ,1.2V)	38	33	37	27

From the results in Table –I we can state the following:

- The proposed vedic multiplier has little bit larger area than array and dadda multiplier but lesser than wallace tree multiplier.
- The vedic multiplier is efficient in terms of delay than other multipliers.
- It is efficient in terms of power dissipation also as shown in the table the results are compared at different supply voltages & frequencies.

5. FUTURE WORK

In present work only one multiplication aspect of Vedic mathematics is touched but there are more formulas needs to be explored like square root, cube root, division. There is further scope to improve implementation of the multiplier presented to reduce the area & Static power dissipation. Multiplication and Division have innumerable applications which can be implemented using Vedic Mathematics. The multiplier proposed can be used for implementation of multiplication of Quadratic equations.

6. CONCLUSION

It is observed that Vedic multipliers are better than other multipliers as compared to the speed & power at 8x8, but has significantly larger area. Power dissipation is reduced for 8x8 bit multiplier by 50% for 20 MHz, 1.2V and 53.44% for 50 MHz, 1.2V. Basis upon the research work done it can be concluded that as the size of multiplication in terms of bits increases the Vedic multiplier shows good performance in terms of speed & power.

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